the first amount of data corresponding to the first block size information; and

providing a first portion of the first amount of data to the memory device synchronously with respect to a first transition of an external clock signal, and a second portion of the first amount of data synchronously with respect to a second transition of the external clock signal.

152. The method of claim 151 further including providing a second block size information to the memory device wherein the second block size information defines a second amount of data to be input by the memory device in response to a second write request.

153. The method of claim 151 further including:

issuing a second write request to the memory device, wherein in response to the second write request the memory device samples a second amount of data corresponding to second block size information; and

providing a first portion of the second amount of data to the memory device synchronously with respect to a third transition of the external clock signal, and a second portion of the second amount of data synchronously with respect to a fourth transition of the external clock signal.

154. The method of claim 151 further including:

issuing a request for a read operation to the memory device, wherein in response to the request for a read operation, the memory device outputs a second amount of data corresponding to second block size information; and

receiving the second amount of data from the memory device.

155. The method of claim 151 wherein the first block size information and the first write request are included in a request packet.

156. The method of claim 155 wherein the first block size information and the first write request are included in the same request packet.

157. The method of claim 151 wherein the data is provided to the memory device after a number of clock cycles of the external clock signal transpires.

158. The method of claim 157 wherein the number of clock cycles is represented by a fraction.

159. The method of claim 151 wherein the first block size information is a binary representation of the first amount of data to be sampled in response to the first write request.

160. The method of claim 151 wherein the first amount of data corresponding to the first block size information is provided synchronously during a plurality of clock cycles of the external clock signal.

161. The method of claim 151 wherein the first transition of the external clock signal is a rising edge transition and the second transition of the external clock signal is a falling edge transition.

162. The method of claim 151 wherein the first and second transitions of the external clock signal transpire during a common clock cycle of the external clock signal.

163. A method of operation of a memory device, wherein the memory device includes a plurality of memory cells, the method of operation of the memory device comprises:

receiving first block size information from a master, wherein the first block size information defines a first amount of data to be sampled by the memory device in response to a write request;

receiving a first write request from the master; and

sampling a first portion of the first amount of data synchronously with respect to a first transition of an external clock signal and a second portion of the first amount of data synchronously with respect to a second transition of the external clock signal.

164. The method of claim 163 wherein the first transition of the external clock signal is a rising edge transition and the second transition of the external clock signal is a falling edge transition.

165. The method of claim 163 further including receiving second block size information from the master, wherein the second block size information defines a second amount of data to be input by the memory device in response to a second write request.

166. The method of claim 163 further including:

receiving a second write request from the master; and

inputting a second amount of data corresponding to second block size information synchronously with respect to a third transition of the external clock signal and a second portion of the first amount of data synchronously with respect to a fourth transition of the external clock signal.

167. The method of claim 166 wherein the third and fourth transitions of the external clock cycle transpire during a common clock cycle of the external clock signal.

168. The method of claim 163 wherein the first block size information and the first write request are included in the same request packet.

169. The method of claim 163 wherein the first block size information is a binary representation of the first amount of data to be input in response to the first write request.

170. The method of claim 163 wherein the first amount of data corresponding to the first block size information is input synchronously during ~~one~~ the same clock cycle of the external clock signal.

171. The method of claim 163 wherein the first amount of data corresponding to the first block size information is sampled synchronously during a plurality of clock cycles of the external clock signal.

172. The method of claim 163 further including generating an internal clock signal using a delay locked loop circuit and the external clock signal wherein the first amount of data corresponding to the first block size information is sampled in response to the internal clock signal.

173. The method of claim 163 further including generating first and second internal clock signals using clock generation circuitry and the external clock signal wherein the first amount of data corresponding to the first block size information is sampled synchronously with respect to the first and second internal clock signals.

174. A method of operation of an integrated circuit device having a synchronous interface, the method of operation of the integrated circuit device comprising:

receiving block size information, wherein the block size information defines an amount of data to be sampled by the integrated circuit device in response to a write request;

receiving a write request; and

sampling a first portion of the amount of data synchronously with respect to a first transition of an external clock signal and a second portion of the amount of data synchronously with respect to a second transition of the external clock signal, wherein the first and second transitions of the external clock signal ~~transpire~~ occur during ~~one~~ the same clock cycle of the external clock signal.

175. The method of claim 174 wherein the first transition of the external clock signal is a rising edge transition and the second transition of the external clock signal is a falling edge transition.

176. The method of claim 174 further including:

receiving a read request; and

outputting a first portion of the amount of data synchronously with respect to a third transition of the external clock signal and a second portion of the amount of data synchronously with respect to a fourth transition of the external clock signal.

177. The method of claim 174 wherein the block size information and the write request are included in the same request packet.

178. The method of claim 174 wherein the block size information is a binary representation of the amount of data to be sampled in response to the write request.

179. The method of claim 174 further including generating an internal clock signal using a delay locked loop and the external clock signal wherein the amount of data corresponding to the block size information is input synchronously with respect to the internal clock signal.--

REMARKS

This Preliminary Amendment seeks to place this application in condition for allowance. This application is a continuation of Application Serial No. 09/252,998, which is a continuation of Application Serial No. 08/979,127, now U.S. Patent 5,915,105. Application Serial No. 09/252,998 is still pending.

Applicants request priority to Application Serial No. 07/510,898, filed April 18, 1990, now abandoned. Applicants request such priority through Application No. 09/252,998, filed on February 19, 1999 (still pending), which is a continuation of Application No. 08/979,127, filed on November 26, 1997 (now U.S. Patent 5,915,105), which is a continuation of Application No.